

Prototype PCB Mill-ability and Element Spacing

The spacing between copper areas on a PCB (tracks, pads, vias, copper pours, etc.) has a big impact on the “mill-ability” of the PCB. Several characteristics of our PCB prototyping system interact, in one way or another, impacting the system. A designer’s choices for spacing parameters have consequences that include:

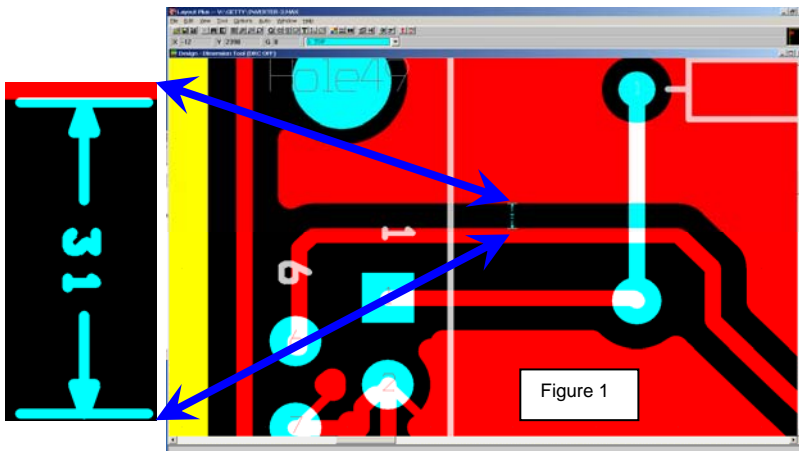
- Tool size – smaller tools are exponentially more expensive to operate
- Machine accuracy – rated to 0.001” (1mil) repeatability, but larger errors can occur
- System memory – can render a design un-millable if objects contain too much detail

Getting parameters set properly in the board layout file is the first step to ensuring that a board can be quickly, completely and repeatably milled without error. The technology files 2X3_1S.tch and 2X3_2S.tch (on \\Gilbert\Micromill\!MSU_Templates\) are single sided and doubled sided templates that have most of the preferred parameters already saved in the file.

One of the confusing areas in OrCAD Layout is the various board parameters that affect spacing to copper pours. In the following series of figures, some of these parameters are adjusted to demonstrate the effect on the shape and spacing of the copper pour. For each figure the critical parameters are provided:

- Track-to-track Spacing (TTTS) [*Options>Global Spacing*]
- Obstacle Width [*Spreadsheet>Obstacles>Copper Pour>Properties>Width*]
- Copper Pour Rules Clearance (CPRC)

TTTS=31mil
OW=31mil
CPRC=0

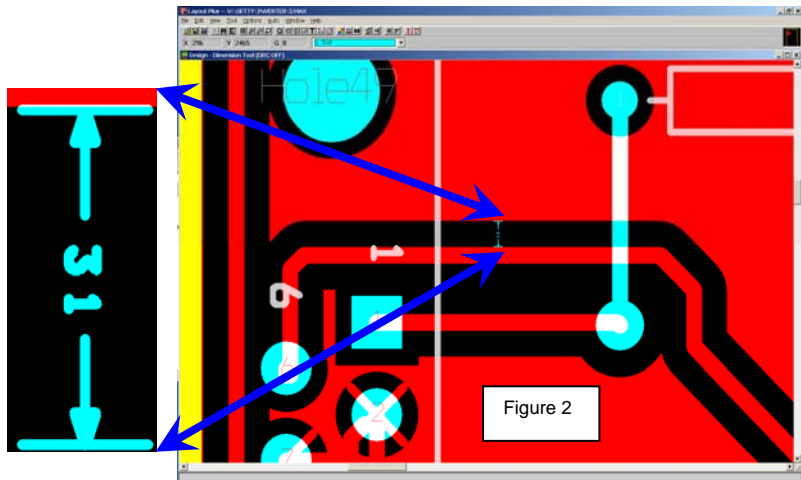


The spacing of the copper pour to other copper entities is controlled in this image (Figure 1) by the recommended minimum TTTS (31mil).

PCB Mill-ability and Element Spacing

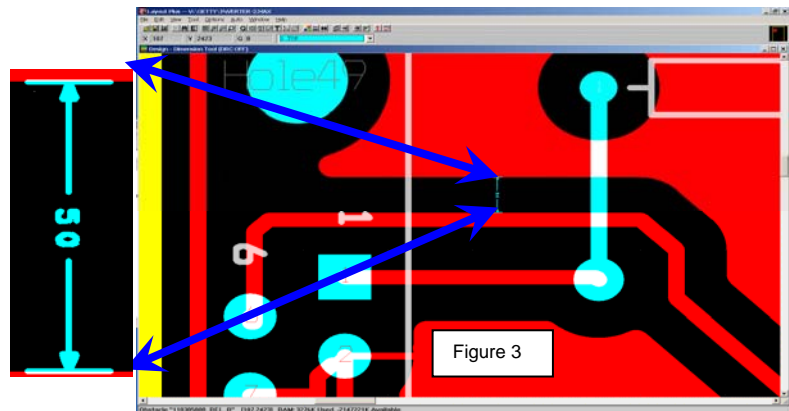
TTTS=31mil
OW=1
CPRC=0

In Figure 2 the copper pour spacing is still controlled by the recommended minimum TTTS (31mil), however the obstacle width (1mil) creates sharp edges and small stubs of copper that consume a lot of memory, at thus a large number of tool movements. This increases substantially the amount of time needed to mill the board and wear on the tools.



TTTS=31mil
OW=31
CPRC=50

In Figure 3 the Copper Pour Rules Clearance (CPRC) value has been set to 50mil (as shown below). In this case, the clearance value was greater than the TTTS setting, so the copper pour spacing was controlled by this CPRC value, not the TTTS as was true in figures 1 and 2. These settings are useful for higher voltage applications (e.g. 120VAC) but involve some tradeoffs. The larger spacing permits the use of larger diameter tooling, but it also requires the removal of additional material. Setting TTTS to 31mil and OW=0mil are suitable for most applications.



PCB Mill-ability and Element Spacing

One parameter that is not set in the technology file is the CPRC parameter. If you use the default 31mil TTTS, the copper pour will be spaced 31mil away from your traces. Only larger spacing between the copper pour and other copper elements on the board require changing the CPRC parameter.

Note also that it is good practice to run “design rules check” on your board before submitting it. That will flag any spacing errors that might have crept into your design.

Obstacle Name: 142

Obstacle Type: Copper pour

Group: Height: Width: 31.

Obstacle Layer: BOTTOM

Copper Pour Rules

Clearance: 50. Z order: 0

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

Isolate all tracks Seed only from designated object

Net Attachment ("-" for none): 0

Do Not Fill Beyond Obstacle Edge

Hatch Pattern.. Comp Attachment..

OK Help Cancel

